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DESIGN AND IMPLEMENTATION OF A MULTIPLE-VALUED LOGIC FPGA BASED ON CONVERT–CODED-COLLECT (CCCI) SPACE THEORY

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ABSTRACT

The Multiple-Valued Logic (MVL) is one of the keys to build the future logic circuits. One of the most important logic units is Field Programming Gate Array (FPGA). Multiple-valued FPGA structures have interconnections less than that in binary FPGAs. Because the inherent dominate delay, power and size the Multiple-valued logic offers overcoming such issues, such as reduction of the number of signals in the circuit.

This Works proposes a new structure of FPGA that based on a new theory of multiple-valued logic (MVL) called Convert-Coded-Collectspace (CCCi). The CCC is paceis a closed space with iinteger values, used to convert the input to output in three phases called convert phase, coded phase, and collect phase, respectively. This paper implement a quaternary FPGA also, it show an example to design a logic multiplexer and flip-flop, under CCC4 space to verify of the new theory for MVL where the two examples are the basic elements of FPGA cells.

KEYWORDS: Multiple Valued Logic, Interconnections, FPGA, CCCi Space, Multiplexer, Flip-Flop